FEATURES

- Implements ATM-25 Mbit/s TC and PMD layer functions

- Supports up to 100 meters of Shielded Twisted Pair (STP) or Unshielded Twisted Pair types 3, 4 or 5 (UTP-3,4,5) cable

- Full Duplex 8-bit data transfers to/from ATM layer protocol chip plus parity

- Integrated FIFO stores up to two 53-byte ATM cells received from network

- Provides data scrambling/descrambling for robust EMC and transmission performance

- Provides 4-bit/5-bit encoding and NRZI format to enable efficient utilization of the channel and reliable clocking

- Provides signal detect logic to determine PLL lock and status of link

- Supports transmission and regeneration of an 8 kHz sync pulse for audio and video applications

- Complies with ATM Forum "ATM 25.6 Mbps Physical Interface Specification"

- Controller (ALI-25C) chip is available in a 68-pin PLCC, uses a single +5 volt supply, and dissipates 280 mW nominal

- Transceiver (ALI-25T) chip is available in a 44-pin PLCC, uses a single +5 volt supply, and dissipates 420 mW nominal. Two versions are available, with high ("A") or low ("B") receiver sensitivity.

DESCRIPTION

The ATM Line Interface 25 Mbit/s (ALI-25) Chip Set provides the complete ATM-25 Physical Layer function including the Transmission Convergence (TC) and Physical Media Dependent (PMD) sub-layers and operates over existing cable plants (STP, UTP-3,4,5). The ALI-25 Chip Set delivers the power of ATM to the desktop at low cost.

Providing both the TC and PMD sub-layer functions, the ALI-25 Chip Set is a key component for system designers developing ATM-25 Mbit/s networking solutions. This Controller/Transceiver chip set has a straightforward system interface which easily connects to available ATM-layer protocol chips such as the SARA-S and the SARA-R (TXC-05501 and 05601) or FIFO designs. The chip set is a total solution for delivering ATM at 25 Mbit/s Physical Layer Network Interfaces over in-house cable plants.

APPLICATIONS

- PC and Workstation Network Interface Adaptors

- ATM Concentrators

- ATM Hubs

- Local and Campus ATM Switches
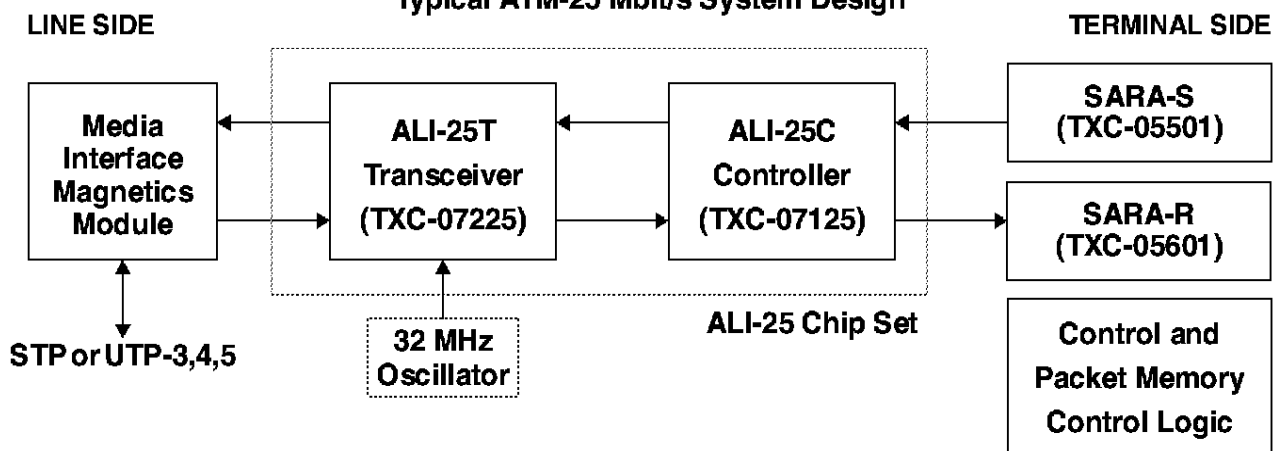
Typical ATM-25 Mbit/s System Design

LINE SIDE

TERMINAL SIDE

Media Interface Magnetics Module

ALI-25T Transceiver (TXC-07225)

ALI-25C Controller (TXC-07125)

SARA-S (TXC-05501)

SARA-R (TXC-05601)

Control and Packet Memory Control Logic

STP or UTP-3,4,5

32 MHz Oscillator

ALI-25 Chip Set

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BLOCK DIAGRAM (ALI-25C)

LINE SIDE **TERMINAL SIDE**

TxDat ← | Serializer NRZ to NRZI |
TxClk ← |

5 → | 4-bit/5-bit Symbol Encoder |
4 → | Transmit Scrambler |
4 → | Transmit Interface |

8 + p
TData(7-0)
TDPrty
TBClk
TDVal
TLoad
TFSyn

Transmit Clock

← Transmit

TxOsc → | Front End Control |
TcSel → |
FrAq ←

Control and Configuration

Reset
Halt_Tx
HEC_Enable
TP_Enable
ICDMode
PowOff

PLL Lock

Sig_Detect ← | Signal Detect Logic |
Sig_Det_Trans ←

Transmit and Receive Error Logic

PErr
CErr
OverRun
EInt
EOE

Receive →

RxDat → | Deserializer NRZI to NRZ |
RxClk →
5 → | 5-bit/4-bit Symbol Decoder |
4 → | Receive Descrambler |
4 → | Receive Interface and FIFO |

8 + p
RData(7-0)
RDPrty
RBClk
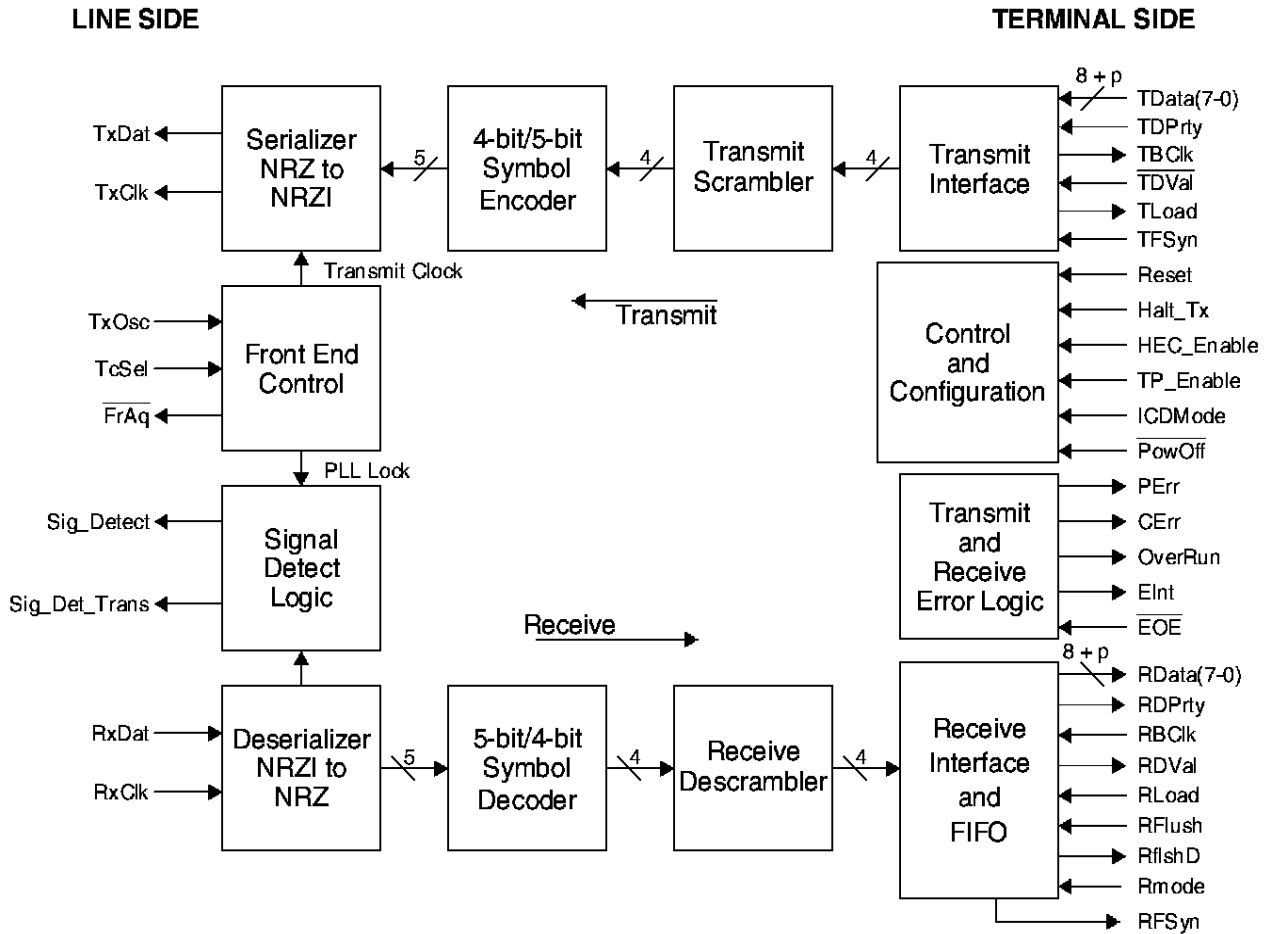RDVal
RLoad
RFlush
RflshD
Rmode
RFSyn

Figure 1. ALI-25C TXC-07125 Block Diagram

BLOCK DIAGRAM DESCRIPTION (ALI-25C)

A simplified block diagram of the ALI-25C is illustrated in Figure 1. The Receive data path takes serial data from the ALI-25T (see Figure 2), converting the data from NRZI to NRZ format and into a parallel 5-bit symbol. The 5-bit symbol is converted into a 4-bit nibble of scrambled data and passed to the receive descrambler. The receive descrambler converts the nibble into 4 bits of data which are the interface control nibbles and data nibbles. The data nibbles are converted into bytes and stored in an output FIFO. Data is then extracted from the receive output by the ATM protocol chip (such as the SARA-R device). Throughout the receive data path, the information contained in the control byte (the first byte of the ATM-25 cell, as described in the Operation section) is used by the various functional blocks to maintain proper operation and data flow.

The serial data signal RxDat and its clock RxClk are converted to 5-bit messages on finding the start of cell message, and sent to the decoder block. The deserializer functional block converts the serial symbols from the ALI-25T chip into 5 bits of parallel data. The NRZI to NRZ format conversion is also performed here. The clocking for this section is provided from the ALI-25T chip, which extracts the clock form the data stream. The 5 bits of parallel data are transferred to the Symbol Decoder (5-bit/4-bit).

The Signal Detect Logic block has two leads that are pinned out of the ALI-25C: The Sig_Detect output is really a "good signal detect" lead since it becomes active when the ALI-25C has determined that a valid ATM-25 signal is being received from the network. The good signal logic also requires that the ALI-25T phase locked loop is indeed in lock. The Sig_Det_Trans output is an "alarm" lead that indicates changes in the Sig_-Detect lead.

The 5-bit / 4-bit Symbol Decoder block converts the 5-bit symbols to scrambled nibble data. The decoder detects the occurrence of the special 5-bit non-data symbol which indicates that this and the subsequent 5-bit signal make up one of the three special mnemonics. The three special mnemonics are used to represent:

• Start of cell with scrambler / descrambler initialized

• Start of cell without scrambler / descrambler initialized

• Timing pulse marker which is used by the receive ALI-25C to generate an 8 kHz synchronization pulse

The decoder then notifies the descrambler that the next 2 nibbles are special control information symbols which need to be processed differently.

The descrambler takes the 4-bit nibbles and descrambles them in exactly the inverse of the manner in which they were scrambled in the transmit side of the ALI-25C device. Both the scrambler and descrambler are reset to their initial state when the special mnemonic indicating "Start of cell with scrambling initialized" is detected. Since the three mnemonics were not scrambled prior to transmission, they are not de-scrambled by the receive descrambler.

The receive interface receives nibbles from the descrambler and turns them into bytes for storing in a FIFO. The FIFO is 2 x 53 bytes deep (2 ATM cells). When a cell is ready, this block coordinates the transfer of the ATM cells to the ATM layer device (SARA-R) and performs all the necessary handshaking to transfer the data between the chips. This block also performs HEC checking (if enabled) and can discard idle cells (if enabled). Neither the control byte nor the random data, which is transferred during idle (non-data) periods, is transferred out of the receive interface. Throughout the receive path, the information contained in the control byte is used by the various functional blocks to maintain proper operation and data flow. For example, the RFSyn lead goes high when a synchronization message is received from the data link.

The RMode pin is used to control the state of the output pins during idle periods.

- RMode low: the drivers are always enabled.

- RMode high: the drivers are hi-Z until there is data to be transferred.

In the Transmit direction, there are 8 data input pins, TData(7-0), plus a parity (odd) bit pin, TDPrty, providing inputs to the Transmit Interface block. The TBClk is an output clock at 3.2 MHz, nominal, to extract the data from the SARA-S or a FIFO. The $\overline{TDVal}$ input pin has a signal which is low for the duration of the cell from the cell source, and the signal on the TLoad pin is an output enable to the connected device. The TFSyn input causes a special timing pulse marker to be sent to the network. It is used for 8 kHz frame synchronization when it is required. The ALI-25C will pass through the HEC.

The transmit scrambler block gets 4-bit nibbles from the transmit interface and converts them into 4 bits of pseudo-random data. The scrambler modifies the mnemonic in the first byte to "start of cell, scrambling initial-ized" if the subsequent cell requires the descrambler to be initialized. The scrambler does not scramble any one of the three possible mnemonics that precede the new cell.

The transmit symbol encoder block takes the input nibbles from the scrambler and converts them into 5-bit symbols. The most important reason for this encoding is to guarantee sufficient data transitions for reliable clock recovery. The second reason is to help identify uniquely the special mnemonics generated by the trans-mit interface block. These nibbles are encoded into non-data 5-bit symbols. This allows the receiver to identify that the current and the next 5-bit symbol are control information and are not a part of the ATM cell itself.

The serializer takes the 5-bit symbols from the symbol encoder and converts them into serial data. The serial data is further converted into a non-return to zero-invert (NRZI) format. The clock to accompany the data is selected by the state of the TcSel lead:

- If TcSel is low, the Transmit Clock is taken from the receive clock on RxClk.

- If TcSel is high, the Transmit Clock is taken from the TxOsc local oscillator input.

The Transmit and Receive Error Logic has four error pins: PErr, CErr, OverRun and Sig_Det_Trans. The latter pin is shown from the Signal Detect Logic, but it is driven from this block. All error output pins are high impedance until EOE (enable output error) is made active. The exception is EInt (error interrupt) which goes high on the event of Sig_Det_Trans (if enabled), CErr (if enabled), PErr, or OverRun.

CErr indicates that a cell error has occurred on the receive side of the ALI-25C.

PErr indicates that a parity error has occurred on the transmit interface from the cell source.

OverRun is an error indicating that a FIFO overflow has occurred on the receiver, e.g. the cell interface did not respond to the RDVal output in time. The Sig_Det_Trans lead represents the logic state of the last change of the Sig_Detect output, which is not latched.

The Control and Configuration block has only input pins. These input pins have the following functions:

- Halt_Tx Low: Normal operation

- Halt_Tx High: TxClk and TxDat are forced low.

HEC_Enable enables HEC checking in the receive interface block when it is high. Further, during Reset:

- HEC_Enable High: interrupt enabled for Sig_Det_Trans changing states.

- HEC_Enable Low: interrupt disabled for Sig_Det_Trans.

TP_Enable enables parity checking on the input of the transmit interface when it is high. Further, during reset:

- TP_Enable High: an interrupt is enabled for CErr when it occurs.

- TP_Enable Low: CErr occurs coincidently (if it is true) with the output on RDVal, and there is no interrupt. If this is to be true, however, the EOE lead must be held low to enable the CErr output driver. During this, the EInt, OverRun, PErr, and Sig_Det_Trans signals are ignored.

ICDMode being low causes idle cells to be transmitted, while ICDMode being high causes idle cells to be discarded as received from the network.

PowOff is normally high for operating the ALI-25C. When it is low, the ALI-25C is powered down.

BLOCK DIAGRAM DESCRIPTION (ALI-25T)

A simplified block diagram of the ALI-25T is illustrated in Figure 2. The ALI-25T device contains many analog circuits and a few digital circuits. The receiver takes in bipolar data, equalizes it to compensate for the line distortion, changes it to unipolar data, recovers clock from the input data, and outputs the clock and data to the ALI-25C device. The transmitter simply takes data from the ALI-25C, converts it to a bipolar format and transmits this on the line side output.

There are two versions of the ALI-25T device. The original version (designated "A", part number TXC-07225-ACPL) has a higher receiver sensitivity than a second alternative version (designated "B", part number TXC-07225-BCPL). These two versions otherwise share all of the characteristics described in this Data Sheet, except where differences between the "A" and "B" versions are specifically identified.

The power and levels of the transmitter output are set by the combination of an on-chip voltage reference and an external bias resistor connected to the RBias pin.

The equalizer section of the Receiver and Equalizer block has two external pins (EQA and EQB) that have an RC circuit between them as part of the equalization. The receiver converts the bipolar input from the transformer into a data signal for the Phase Locked Loop block. The data output goes both to the output latch and to the Phase Locked Loop for clock recovery. The receiver also detects the signal amplitude and disables the receiver path if the signal is too low.

The phase locked loop (PLL) block requires an RC circuit connected between PLLFLT and PLLFLTG as part of the PLL. When the ALI-25T is powered-up, the FrAq lead is made active. This causes the 32 MHz crystal input Xtal to be used to center the internal VCO at the nominal point to give the normal operating frequency of 32 MHz. The recovered clock is used to clock out the data from the output latch.

The loopback block is enabled by the $\overline{\text{FEWrap}}$ lead being active. This lead also disables the Transmitter Block, and, of course, the receive input data is blocked by the loopback data. The ALI-25C sends and receives the data, while the ALI-25T is isolated from the line side facility.

The latch and buffer blocks provide the outputs to the ALI-25C device. The RxDat and the recovered clock, RxClk, are the cell output data and clock. The TxOsc output is a buffered equivalent of the Xtal input signal, which is required to be provided by a 32 MHz crystal. This can form the reference transmit frequency for the ALI-25C.

BLOCK DIAGRAM (ALI-25T)
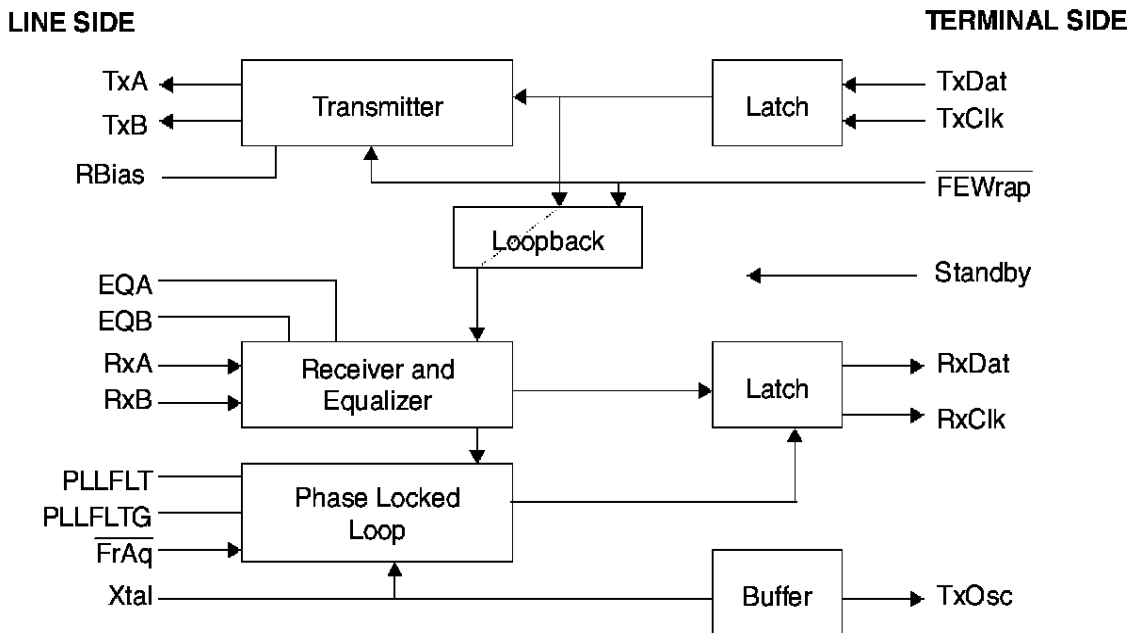
Figure 2. ALI-25T TXC-07225 Block Diagram

PIN DIAGRAM (ALI-25C)

TLoad	10	60 PErr
RData 0	11	59 Vdd
RData 1	12	58 $\overline{EOE}$
RData 2	13	57 TxClk
RData 3	14	56 Halt_Tx
GND	15	55 GND
Vdd	16	54 RxClk
RBClk	17	53 GND
GND	18	52 RxDat
TBClk	19	51 GND
GND	20	50 TxDat
Vdd	21	49 $\overline{FrAq}$
TData 3	22	48 Reset
TData 2	23	47 RFlush
TData 1	24	46 RMode
TData 0	25	45 ICDMode
$\overline{TDVal}$	26	44 Sig_Detect

Top: 9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61

ALI-25C (Top View)

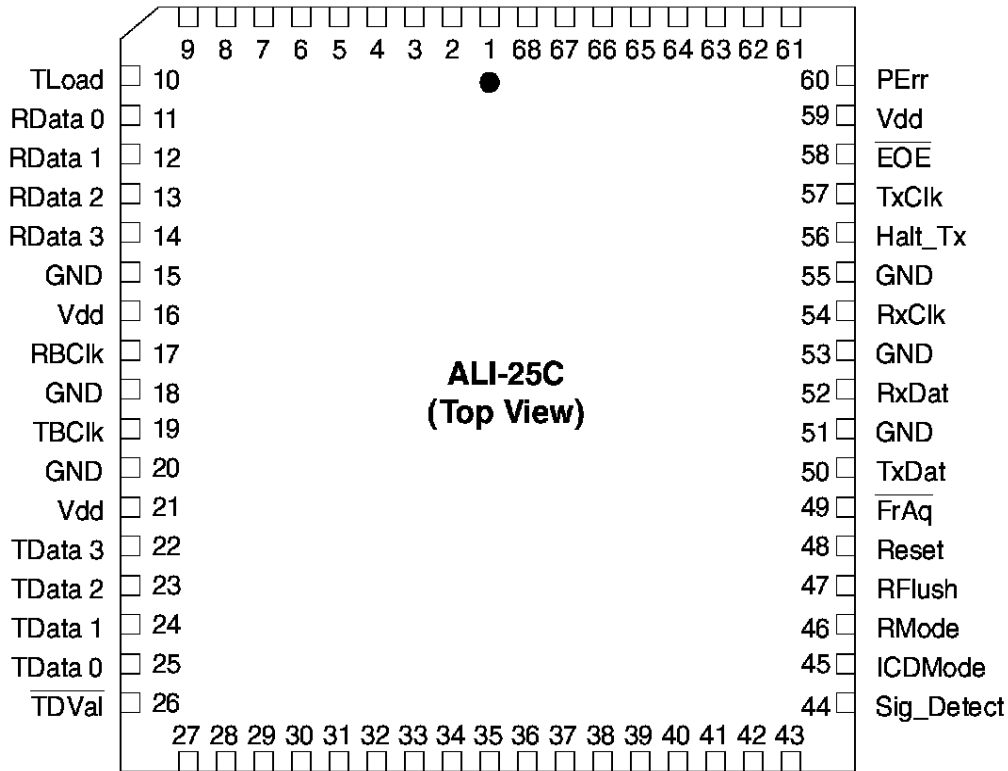Bottom: 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43

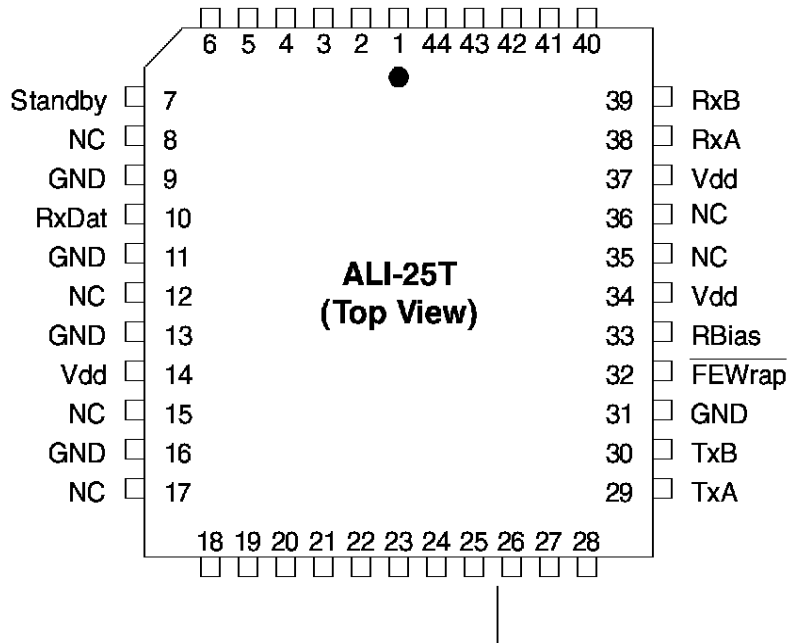Figure 3. ALI-25C TXC-07125 Pin Diagram

PIN DIAGRAM (ALI-25T)

Figure 4. ALI-25T TXC-07225 Pin Diagram

PIN DESCRIPTIONS (ALI-25C)

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
Vdd	16, 21, 34, 59, 68	P		**Vdd**: +5-volt supply voltage, ±5%
GND	1, 15, 18, 20, 35, 51, 53, 55	P		**GND**: Ground

* Note: I = Input, O = Output, P = Power

Spares

Symbol	Pin No.	I/O/P	Type	Name/Function
NC	37 - 42			**No Connection**: These pins are typically special input and output pins used during the manufacturing test and diagnostics of the wafer die and module. These pins must not be connected to anything in the board level design. *They must be left open.*

Transmit and Receive Interface between ALI-25C and ALI-25T

Symbol	Pin No.	I/O/P	Type*	Name/Function
RxDat	52	I	TTL	**Receive Data**: Serial data input from the ALI-25T that is sampled by the recovered clock.
RxClk	54	I	TTL	**Receive Clock**: Recovered clock from the ALI-25T.
$\overline{\text{FrAq}}$	49	O	TTL2mAz	**Frequency Acquisition**: When the ALI-25C detects that the receive clock / data is out of specification, it causes this lead to be active (low) toward the ALI-25T to cause it to re-acquire the PLL with the external 32 MHz clock.
TxDat	50	O	TTL2mAz	**Transmit Data**: Serial, encoded, scrambled data output to the ALI-25T.
TxClk	57	O	TTL2mAz	**Transmit Clock**: Transmit clock used by the ALI-25T to sample the output data, TxDat.
TxOsc	36	I	TTL	**Transmit Oscillator**: Local crystal oscillator input from the ALI-25T.
TCSel	9	I	TTL	Transmit Clock Select: Select the clock to be used for transmit operation: • Low = RxClk is used (loop timing) • High = TxClk is derived from the local oscillator on the TxOsc lead.

*See Input, Output and I/O Parameters section for Type definitions.

Terminal Side Receive Data

Symbol	Pin No.	I/O/P	Type	Name/Function
RData (7-4) RData (3-0)	32-29 14-11	O	TTL2mAz	**Receive Data**: Eight-bit parallel data ATM cell output to the ATM layer protocol chip. Bit 7 is the most significant bit.
RBClk	17	I	TTL	**Receive Byte Clock**: Input clock from ATM layer protocol chip to transfer data from the ALI-25C. Maximum clock rate = 20 MHz.
RDPrty	33	O	TTL2mAz	**Receive Data Parity**: Odd parity bit over the output data on RData (7-0).
RMode	46	I	TTLd	**Receive Mode**: The state of this input controls the mode of operation of the receive data output: • Low = Data output drivers always enabled • High = Output drivers in high impedance mode (Hi-Z) until RLoad is asserted.
RDVal	28	O	TTL2mAz	**Receive Data Valid**: Output during the ATM cell transfer indicating the presence of the cell.
RLoad	27	I	TTL	**Receive Load**: Input from ATM layer protocol chip enabling data transfer from the ALI-25C. If RLoad is de-asserted during cell transfer, the ALI-25C suspends its output at a byte boundary. The next byte of the cell is enabled when RLoad is re-asserted.
RFlush	47	I	TTL	**Receive (FIFO) Flush**: When this pin becomes active from the ATM layer protocol chip, it causes the ALI-25C to drop all cell data in its output FIFO.
RFlshD	7	O	TTL2mAz	**Receive (FIFO) Flush Done**: The signal on this pin becomes active from the ALI-25C indicating that the flush command on pin 47 is complete.

Terminal Side Transmit Data

Symbol	Pin No.	I/O/P	Type	Name/Function
TData (7-4) TData (3-0)	3-6 22-25	I	TTL	**Transmit Data**: Eight-bit parallel data ATM cell input from the ATM layer protocol chip. Bit 7 is the most significant bit.
TBClk	19	O	TTL2mAz	**Transmit Byte Clock**: Output clock from the ALI-25C to transfer data from the ATM layer protocol chip. It is typically at 3.2 MHz.
TDPrty	2	I	TTL	**Transmit Data Parity**: Odd parity bit over the input data on TData (7-0).
TDVal	26	I	TTL	**Transmit Data Valid**: Active low input during the ATM cell transfer indicating the presence of the cell.
TLoad	10	O	TTL2mAz	**Transmit Load**: Output signal enabling data, TData (7-0), from the ATM layer protocol chip.

Frame Synchronization Pulses

Symbol	Pin No.	I/O/P	Type	Name/Function
RFSyn	8	O	TTL4mAz	**Receive Frame Synchronization**: The ALI-25C puts a signal on this pin when it receives a timing pulse marker mnemonic from the network.
TFSyn	67	I	TTLd	**Transmit Frame Synchronization**: When the ALI-25C receives a signal on this pin, it sends the timing pulse marker mnemonic to the network. This is used to send an 8 kHz framing indicator.

Transmit and Receive Status / Error Indicators

Symbol	Pin No.	I/O/P	Type	Name/Function
Sig_Detect	44	O	TTL2mAz	**Signal Detect**: An unlatched output indicating that the ALI-25C has determined that a valid ATM-25 signal is being received from the network.
PErr	60	O	TTL4mAz	**Parity Error**: When a parity error is detected on the transmit data input from the ATM layer protocol chip, then PErr is active. The output is high impedance until $\overline{EOE}$ is asserted.
CErr	62	O	TTL4mAz	**Cell Error**: This output is active when the ALI-25C finds an error in the receive cell or in the output FIFO. The output is in a high impedance state until $\overline{EOE}$ is asserted provided that CErr is configured to generate an interrupt on EInt. Otherwise, CErr will be asserted coincident with RDVal of the cell with the error. Configuration is controlled by pin 65, TP_Enable, during reset.
OverRun	64	O	TTL4mAz	**OverRun**: The ALI-25C generates a signal on this lead when its output FIFO is overrun with data. The output is high impedance until $\overline{EOE}$ is asserted.
Sig_Det_Trans	66	O	TTL4mAz	**Signal Detect Transition**: This output indicates that the state of the output pin Sig_Detect has changed. The output is in a high impedance state until $\overline{EOE}$ is asserted. This lead can be masked such that it does not cause an interrupt (see pin 63, HEC_Enable).
EInt	61	O	TTL4mAz	**Error Interrupt**: This error signal is the logical OR of the receiver error signals: Sig_Det_Trans, CErr, PErr, and OverRun.
$\overline{EOE}$	58	I	TTLd	**Error Output Enable**: The signal on this lead enables the receive error output drivers for Sig_Det_Trans, CErr, PErr, and OverRun. This signal clears the error registers on transition from active to inactive.

Configuration Control

Symbol	Pin No.	I/O/P	Type	Name/Function
Halt_Tx	56	I	TTLd	**Halt Transmission**: This pin can set the line side TxDat and TxClk pins low to disable transmission. • Low = Transmit enabled, normal operation • High = Transmit disabled
HEC_Enable	63	I	TTLu	**Header Error Check Enable**: During normal operation, this signal causes HEC verification to be performed on the received cell headers. Invalid HECs will generate cell errors (CErr). During reset, the state of this pin determines if an error interrupt is generated with the Sig_Det_Trans (see Figure 7). • Low = No interrupt generated • High = Interrupt generated on EInt
TP_Enable	65	I	TTLd	**Transmit Parity Enable**: During normal operation, this signal causes parity to be checked on the incoming transmit data. Parity errors will generate a signal on PErr. During reset, the state of this pin determines if ATM cell errors will generate an interrupt on EInt or cause the error to go out with the data (see Figure 7). • Low = CErr coincident with RDval (pin 28) • High = CErr causes interrupt on EInt.
ICDMode	45	I	TTLu	**Idle Cell Discard Mode**: The state of this pin determines the handling of idle cells (VP/VC set to zero). • Low = Idle cells will be transferred • High = Idle cells will be discarded
PowOff	43	I	TTLu	**Power Off**: The state of this pin controls the power-down mode of the ALI-25C. • Low = Chip in power down mode • High = Normal operating mode
Reset	48	I	TTL	**Reset**: Resets the ALI-25C and initializes the connected ALI-25T chip. • Low = Normal operating mode • High = Reset ALI-25C and initialize the ALI-25T

PIN DESCRIPTIONS (ALI-25T)

Power Supply and Ground*

Symbol	Pin No.	I/O/P	Type	Name/Function
Vdd	14, 18, 23, 34, 37	P		**Vdd**: +5-volt supply voltage, ±10%
GND	4, 9, 11, 13, 16, 22, 31	P		**GND**: Ground
AVdd	43	P		**AVdd**: Analog +5-volt supply voltage, ±10%
AGND	44	P		**AGND**: Analog Ground

*Note: see power supply decoupling guidelines section.

Spares

Symbol	Pin No.	I/O/P	Type	Name/Function
NC	3, 5, 8, 12, 15, 17, 21, 27, 28, 35, 36, 40			**No Connection**: These pins are typically special input and output pins used during the manufacturing test and diagnostics of the wafer die and module. These pins must not be connected to anything in the board level design. *They must be left open.*

Line Side Transmit and Receive

Symbol	Pin No.	I/O/P	Type**	Name/Function
TxA, TxB	29, 30	O	Az	**Transmit A, Transmit B**: These pins provide a differential pair with high current outputs to drive a line transformer.
RxA, RxB	38, 39	I	A	**Receive A, Receive B**: These pins provide a differential pair to receive signals from a line transformer. These pins have a DC bias level of Vdd/2 and should not be loaded with a DC path to ground. Normal connection of these pins is through the transformer coupling.

Line Side Analog Component Connections (See Figure 9)

Symbol	Pin No.	I/O/P	Type	Name/Function
RBias	33		A	**Resistor Bias**: A resistor is connected and used in conjunction with an internal band gap reference to generate an accurate reference for receiving data.
EQA, EQB	41, 42		A	**Equalizer A, Equalizer B**: Connections for the on-chip line equalization.
PLLFLT*	1		A	**Phase Locked Loop Filter**: Components for the PLL filter are connected to this pin.
PLLFLTG*	2		A	**Phase Locked Loop Filter G**: Dedicated current return for the PLL.

* These two pins are sensitive to noise and require care in layout of their connecting traces.
**See Input, Output and I/O Parameters section for Type definitions.

Transmit and Receive Interface between ALI-25T and ALI-25C

Symbol	Pin No.	I/O/P	Type	Name/Function
RxClk	6	O	TTL2mAz	**Receive Clock**: This is the clock signal derived from the input data. It is used to clock data into the line side of the ALI-25C.
RxDat	10	O	TTL2mAz	**Receive Data**: This is serial data signal timed by the receive clock and sent to the ALI-25C.
TxClk	19	I	TTL	**Transmit Clock**: This is the clock signal from the ALI-25C used to clock in the transmit data.
TxDat	20	I	TTL	**Transmit Data**: This is the data from the ALI-25C that is to be transmitted to the line side output.
Xtal	25	I	TTL	**Crystal**: A 32 MHz crystal oscillator is required to be connected to this pin.
TxOsc	24	O	TTL2mAz	**Transmit Oscillator**: This is a buffered output of the crystal oscillator that is connected to the ALI-25C chip.

Control and Configuration

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{FrAq}}$	26	I	TTL	**Frequency Acquisition**: When this pin is asserted from the ALI-25C, the ALI-25T uses the crystal oscillator input to center its internal VCO. • Low = Frequency Acquisition • High = Normal Operation
Standby	7	I	TTL	**Standby**: When this pin is asserted, it causes the ALI-25T to go into standby or power-down mode. • Low = Normal operation • High = Standby / power-down mode
$\overline{\text{FEWrap}}$	32	I	TTL	**Wrap**: This pin causes the transmitted signal from the ALI-25C to be looped back from the ALI-25T to the ALI-25C. The transmit output pins (TxA, TxB) are tristated when this pin is asserted. • Low = Loopback enabled, outputs are tristated • High = Normal operation

ABSOLUTE MAXIMUM RATINGS (ALI-25C)*

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vdd	-0.3	+7.0	V
DC Input Voltage	Vin	-0.5	Vdd+0.3	V
Continuous power dissipation	Pc		362	mW
Ambient operating temperature	T_A	0	70	°C
Operating junction temperature	T_J		100	°C
Storage temperature range	T_S	-40	125	°C

ABSOLUTE MAXIMUM RATINGS (ALI-25T)*

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vdd	-0.3	+7.0	V
DC Input Voltage	Vin	-0.5	Vdd+0.5	V
Continuous power dissipation	Pc		550	mW
Ambient operating temperature	T_A	0	70	°C
Operating junction temperature	T_J		100	°C
Storage temperature range	T_S	-55	150	°C

* Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS (ALI-25C)

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient		45		°C/W	0 ft/min airflow

THERMAL CHARACTERISTICS (ALI-25T)

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient		45		°C/W	0 ft/min airflow

POWER REQUIREMENTS (ALI-25C)

Parameter	Min	Typ	Max	Unit	Test Conditions
Vdd	4.75	5.0	5.25	V	
Idd		56	67	mA	
Pdd		280	362	mW	Inputs switching

POWER REQUIREMENTS (ALI-25T)

Parameter	Min	Typ	Max	Unit	Test Conditions
Vdd	4.5	5.0	5.5	V	
Idd		84	100	mA	
Pdd		420	550	mW	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters for TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.2			V	$4.75 \leq Vdd \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq Vdd \leq 5.25$
Input leakage current	-10		10	μA	
Input capacitance		3.5		pF	

Input Parameters for TTLu and TTLd

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.2			V	$4.75 \leq Vdd \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq Vdd \leq 5.25$
Input leakage current	-200		200	μA	
Input capacitance		3.5		pF	

Note: TTLu has an internal nominal 100K pull up resistor. TTLd has an internal nominal 100K pull down resistor.

Output Parameters for TTL2mAz

Note: The TTL2mAz output can be placed into a high impedance, non-operational mode.

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	Vdd = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	Vdd = 4.75; I_{OH} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	5	10	15	ns	C_{LOAD} = 14pF
t_{FALL}	2	4	6	ns	C_{LOAD} = 14pF

Output Parameters for TTL4mAZ

Note: The TTL4mAz output can be placed into a high impedance, non-operational mode.

| Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	Vdd = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	Vdd = 4.75; I_{OH} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.5	5.5	10	ns	C_{LOAD} = 35pF
t_{FALL}	1	2	4	ns	C_{LOAD} = 35pF

Analog I/O Pins (A, Az)

There are analog I/Os on the ALI-25T device that are generally variable in their characteristics. These are designated by the letter A or Az. The Az leads can be placed into a high impedance, non-operational mode.

TIMING CHARACTERISTICS

Detailed timing diagrams for the ALI-25C are illustrated in Figures 5 through 8 with values of the timing intervals following each figure. All output times are measured with a maximum of 14 pF load capacitance. Timing parameters are measured at $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

The interface between the ALI-25C and the ALI-25T is not detailed since the devices are intended to be used together as a chip set. The two devices have adequate margins built into the interface timing so long as the advice given in the Physical Design and Wiring Guidelines sections is followed.

Figure 5. Terminal Side Cell Input of ALI-25C - for Cell Transmission
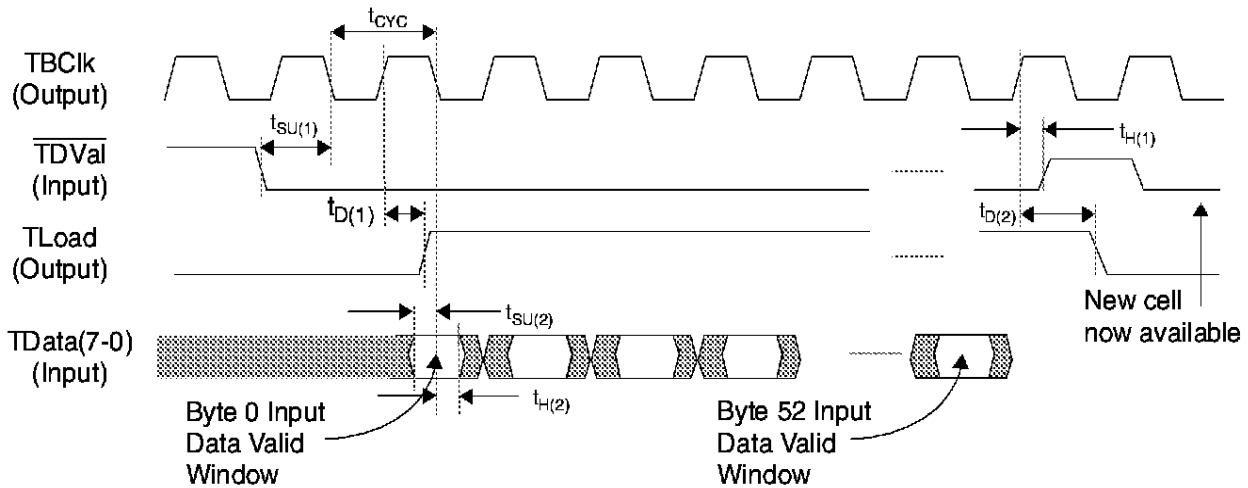
Note: A description of the normal data transfer operation is provided in the ALI-25C Transmit Data Interface subsection of the Operation section below.

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle time of TBClk	t_{CYC}		312		ns
Setup time from TDVal low to TBClk ↓	$t_{SU(1)}$	94			ns
Hold time from TBClk ↑ to TDVal high	$t_{H(1)}$	0			ns
Delay from TBClk ↑ to TLoad high	$t_{D(1)}$		156	188	ns
Delay from TBClk ↑ to TLoad low	$t_{D(2)}$		156	188	ns
Setup time from TData valid to TBClk ↓	$t_{SU(2)}$	94			ns
Hold time from TBClk ↓ to TData invalid	$t_{H(2)}$	32			ns

Note: If the ALI-25C is requested to send the 8 kHz synchronization marker (TFSyn asserted) during the transfer of an ATM cell, then the ALI-25C interrupts the cell transfer for one cycle of TBClk in order to transmit the special mnemonic to its line side output. To interrupt the transmit data interface, the ALI-25C de-asserts the TLoad signal so that the cell transmission is stopped until the ALI-25C reasserts the TLoad signal. The $t_{D(1)}$ and $t_{D(2)}$ times are still valid for this interruption in the TLoad signal.

## Figure 6. Terminal Side Cell Output of ALI-25C - for Cell Reception

RBClk (Input)
RDVal (Output)
RLoad (Input)
RData(7-0) (Output)

Byte 0 Output Data Valid Window

Byte 52 Output Data Valid Window

Byte 0 Output New Cell Data Valid Window
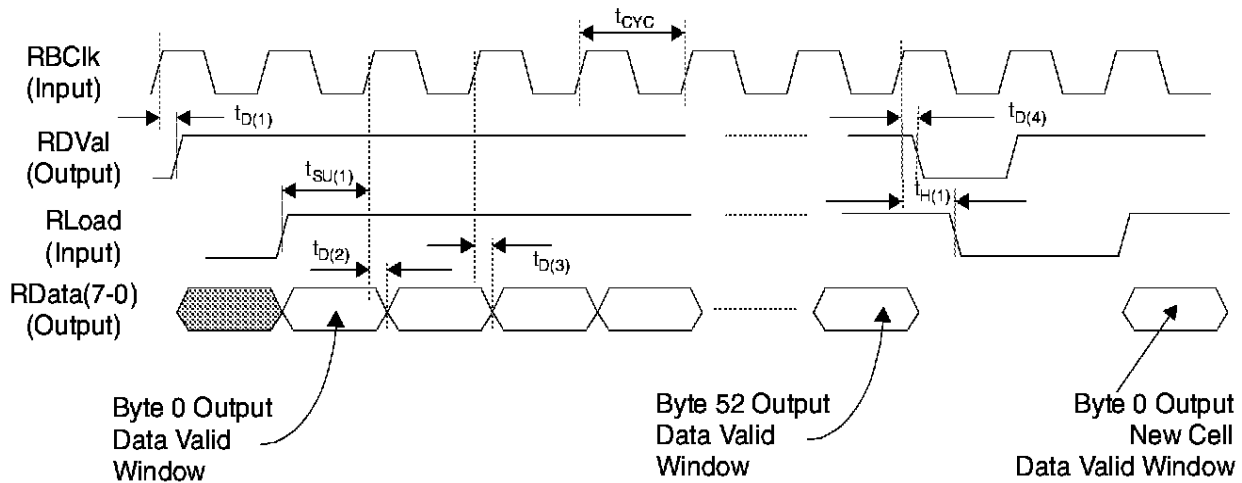
Note: A description of the normal data transfer operation is provided in the ALI-25C Receive Data Interface subsection of the Operation section below.

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle time of RBClk	t_{CYC}	50			ns
Delay time from RBClk ↑ to RDVal high	$t_{D(1)}$		17	31	ns
Setup time from RLoad high to RBClk ↑	$t_{SU(1)}$	20*		t_{CYC} - 10	ns
Hold time from RBClk ↑ to RLoad low	$t_{H(1)}$	10			ns
Delay time from RBClk ↑ to RData valid	$t_{D(2)}$		27**	46	ns
Delay time from RBClk ↑ to RData invalid	$t_{D(3)}$	8	22		
Delay time form RBClk ↑ to RDVal low	$t_{D(4)}$		20	34	

* Note 1: (See the table for Terminal Side Receive Data, RMode, pin 46, in the Pin Descriptions section). The setup time from RLoad high to RBClk↑ assumes that RMode is asserted (high), thus giving a long setup time. This allows for the drivers to come out of the high impedance state with a time of 10 ns (typical) / 20 ns (maximum). At the end of data transmission, the drivers return to the high impedance state within 10 ns (typical) / 20 ns (maximum). When RMode is de-asserted, and the data is immediately available, the required setup time is reduced from 20 to 6 nanoseconds.

** Note 2: The delay time from RBClk rising edge to the data output being valid is true for bytes 1 through 52. Byte 0 is influenced by the state of RMode as explained in Note 1.

Figure 7. Reset Timing and Reset Configuration Timing
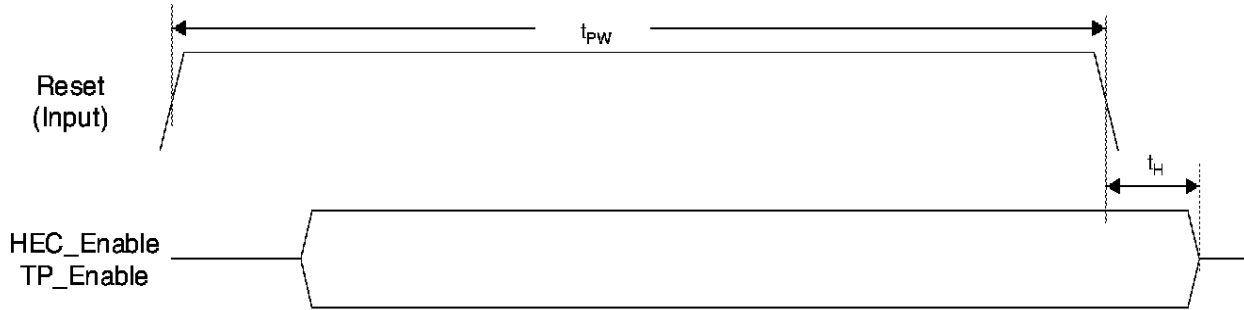
Parameter	Symbol	Min	Typ	Max	Unit
Minimum time for Reset to be valid	t_{PW}	200			ns
Hold time from Reset $\downarrow$ to Enable invalid	t_H	32			ns

Figure 8. Timing for Error Status Reporting
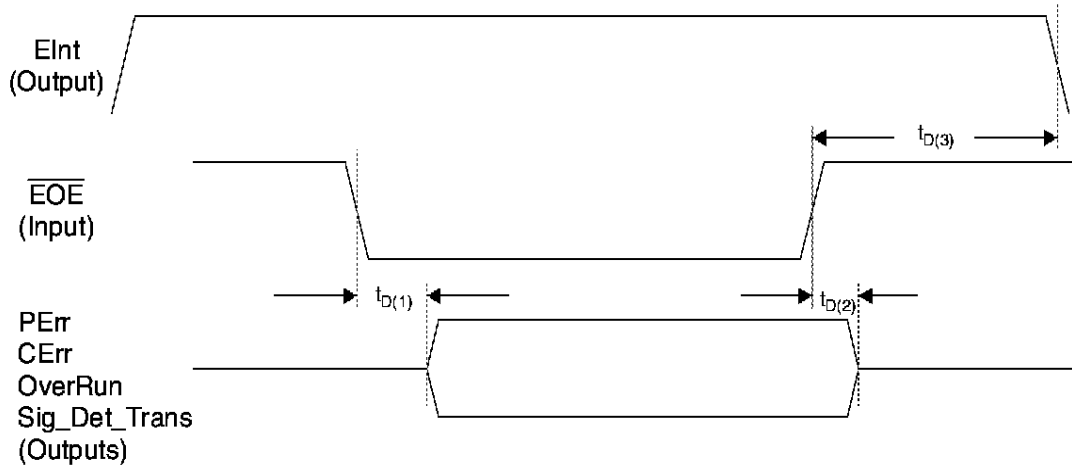
Parameter	Symbol	Min	Typ	Max	Unit
Delay from EOE ↓ to status/error valid	$t_{D(1)}$			25	ns
Delay from EOE ↑ to status/error invalid	$t_{D(2)}$	0			ns
Delay from EOE ↑ to EInt ↓	$t_{D(3)}$			3 cycles of RBClk	ns

Synchronization Pulse Input

The signal on the TFSyn lead (pin 67) is positive edge triggered and the positive pulse width must be greater than 400 nanoseconds.

Synchronization Pulse Output

When the ALI-25C receives the mnemonic representing the timing pulse marker, the ALI-25C puts out a high pulse on RFSyn (pin 8) that is typically 470 nanoseconds wide.

OPERATION

ALI-25C

General

The ATM cell I/O of the ALI-25C is a FIFO-like byte-wide interface with standard control signals and parity on both transmit and receive. The transmitted cell from the ALI-25C has the following format:

Standard ATM Cell	Header 5 bytes	ATM Cell Payload 48 bytes

Control/Information Byte → | ATM Cell, 53 bytes |
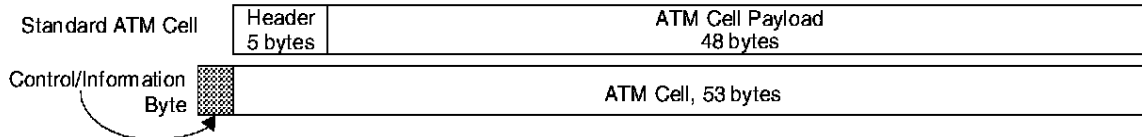
The ALI-25C scrambles all but the Control/Information byte and encodes the data in a 4-bit/5-bit format for transmission by the ALI-25T. Note that the data rate is 3.2 x 8 = 25.6 Mbit/s. The 4-bit/5-bit format makes this

(5/4) x 25.6 = 32 Mbit/s.

The ALI-25C receiver inverts the process of the transmitter and provides access to alarm and control pins to the attending software. It provides a byte-wide output that contains the cells of data in the standard ATM format. The byte clock is 3.2 MHz or one tenth of the 32 MHz crystal oscillator that is required for both the ALI-25C and the ALI-25T. The actual data rate is then 3.2 x 8 = 25.6 Mbit/s, and this has been "shortened" to 25 in this data sheet.

On power-up, or on loss of receive data or clock, the ALI-25C signals the ALI-25T to go into the frequency acquisition mode and lock onto the 32 MHz crystal input.

Transmit Data Interface

The Transmit Data Interface is a 9-bit (data byte plus optional odd parity) unidirectional data bus from the terminal system (ATM Layer Protocol Chip) to the ALI-25C chip. There are three control lines which provide the handshaking between the ALI-25C chip and the system: TDVal, TLoad, and TBClk.

Normal data transfers operate as follows:

1. The system puts the first byte on the data bus and requests to initiate transfer of ATM cell data to the ALI-25C by asserting the TDVal input signal. This signal must stay low for the entire 53-byte ATM cell.

2. The ALI-25C asserts the TLoad output signal to indicate that it is ready to receive the ATM cell data, and receives Byte 0.

- **Note:** The ALI-25C will not always respond with the TLoad signal in the clock cycle immediately following the assertion of TDVal. If TFSyn is active, concurrently with TDVal, then the Tload signal will be delayed by a TBClk clock cycle while the ALI-25C transmits the special mnemonic for the sync pulse.

3. Byte transfer continues on the falling edges of Transfer Clock TBClk.

- **Note:** TBClk is generated by the ALI-25C and is typically 3.2MHz (a divide by 10 of either the local 32MHz oscillator or the recovered clock).

4. The system continues to transfer bytes until a complete ATM cell (53 bytes) has been transferred. Note that the ALI-25C does not buffer the ATM cell but immediately transmits it to the network.

- **Note:** If the ALI-25C is requested to send the timing marker (i.e., if TFSyn input transitions low to high), then the transmit data interface will be interrupted for one TBClk

cycle while the timing marker is transmitted. The ALI-25C will de-assert Tload to interrupt the data transfer and reassert TLoad when the data transfer is ready to continue. When the transfer is interrupted, the system must hold the current data byte until the data transfer begins again.

5. After the system has completed the ATM cell transfer, it must de-assert the TDVal input signal.

6. The ALI-25C responds by de-asserting the TLoad signal.

7. The ALI-25C chip is now ready to receive a second cell (if available)

The Transmit Data Interface timings are shown in Figure 5.

Receive Data Interface

The Receive Data Interface is a 9-bit (data byte plus odd parity) unidirectional data bus from the ALI-25C chip to the terminal system (ATM Layer Protocol Chip). There are three control lines which provide the handshaking between the ALI-25C chip and the system: RDVal, RLoad, and RBClk.

Normal data transfers operate as follows:

1. When a complete ATM cell is stored in its FIFO, the ALI-25C puts data Byte 0 on the bus and requests to initiate cell data transfer by asserting the RDVal signal.

   - **Note:** If RMode is low, the drivers are always enabled. If RMode is high, then the drivers remain in high-Z mode until the RLoad signal is asserted.

2. The system must respond by asserting the RLoad signal. The system may assert RLoad in the same RBClk clock cycle that the ALI-25C asserts RDVal, or in any subsequent RBClk cycle.

3. Byte transfer begins on the rising edge of the Transfer Clock RBClk.

   - **Note:** RBClk is provided by the ATM Layer Protocol Chip and can have a maximum clock rate of 20MHz.

   - **Note:** The Parity bit is only valid when the signal RDVal is asserted.

4. The system continues to transfer bytes until a complete ATM cell is transferred (53 bytes).

5. If the ALI-25C detects that RLoad is de-asserted during the cell transfer, the transfer is suspended and will resume at the **next** byte of the cell when RLoad is re-asserted.

6. Once all 53 bytes have been transferred from the FIFO, then the ALI-25C de-asserts the RDVal signal.

7. The system must respond by de-asserting the RLoad signal.

8. This procedure continues as long as there are complete ATM cells stored in the FIFO.

During the normal data transfer it is possible for the ATM Layer Protocol Chip to stop the transfer of the current cell and flush the entire contents of the ALI-25C FIFO. This feature can be used by the ATM Layer Protocol Chip to discard cells which contain errors or are not needed by the system.

The procedure to flush the contents of the FIFO is as follows:

1. The RFlush signal is asserted.

2. All cell data will then be flushed from the FIFO.

   - **Note:** Any cell being received from the network during this time will also be discarded.

3. The ALI-25C will assert RFlshD to indicate that the FIFO has been flushed.

The Receive Data Interface timings are shown in Figure 6.

ALI-25T

The ALI-25T transmits data as it receives it from the ALI-25C, but it converts the NRZI data to symmetric data. This means that the data at TxA is inverted with respect to the data on TxB, thus providing a balanced signal to the output transformer.

It likewise receives a symmetric signal from the input transformer and converts it to a single-ended data signal for recovering the clock from it.

Magnetics Module

The Magnetics Module for the media interface is a hybrid package that contains the input and output transformers and some line equalization components that adapt to the wide range of possible impedances in typical applications. This component is available from Pulse Engineering, Inc. as part number PE-67583 (call 619-674-8100 for information).

The rest of this section explains the connections among these components and gives some guidelines on board layout that can help in optimizing performance with respect to EMI, crosstalk, and noise.

Operational Modes

Standby / Power Down Mode

When the $\overline{\text{PowOff}}$ lead (pin 43 of ALI-25C) is held low and / or the Standby lead (pin 7 of ALI-25T) is held high, the output drivers of the device are placed in a high impedance state and the power is significantly reduced.

Normal Mode

With $\overline{\text{PowOff}}$ held high and Standby held low, the chips are powered up and can be active. In this mode, either ATM cells or idle code is transmitted and received over the network.

Loopback Mode

When the $\overline{\text{FEWrap}}$ lead (pin 32 of the ALI-25T) is driven low by some external control, then the ALI-25C transmitted signal is looped back to the ALI-25C receiver via the looped path in the ALI-25T. The line side output of the ALI-25T is put into the high impedance state. All other control leads are normal except that the TCSel (Transmit Clock Select, pin 9 of the ALI-25C) lead must be held high in order to select the 32 MHz input as the transmit reference clock.

Initialization

The ALI-25 Chip Set must be initialized after power-up or after a return from the power-down mode. The Reset signal on the ALI-25C controls the initialization. Initialization is not required when switching to / from the loop-back mode.

Prior to initialization, the $\overline{PowOff}$ pin on the ALI-25C must be high or disconnected and the Standby pin on the ALI-25T must be held low. In addition, both devices must have a valid 32 MHz clock input present (Xtal for ALI-25T, TxOsc for ALI-25C, as shown in Figure 9) and the ALI-25C must have a valid RBClk input present.

To initialize, the Reset pin on the ALI-25C must be asserted for a minimum of 200 nanoseconds (see Figure 7). The ALI-25C is immediately configured for normal operation. The ALI-25C asserts the $\overline{FrAq}$ signal to the ALI-25T which causes it to lock onto the local 32 MHz oscillator. Once the PLL lock has been established, the ALI-25C switches the ALI-25T back to normal (phase detect) mode. The ALI-25C then uses the good signal detect algorithm to monitor the received data and determine if a valid ATM 25 Mbit/s signal exists. Once it has determined that a valid signal exists, the Sig_Detect pin goes high. The Chip Set takes between 224 and 288 microseconds to detect the existence of a valid signal.

After the reset initialization is complete, the ALI-25C and ALI-25T chips can optionally be placed in loopback to perform a diagnostic check.

During reset, the ALI-25C clock and data signals are held low so that no data is transmitted to the network by the ALI-25T. In this way, the receiving ALI-25T has no trouble in recovering the clock. After reset, the ALI-25C automatically transmits idle pseudo-random data. Should the ALI-25C receive pseudo-random data, it discards it since it is not in the standard ATM 53-byte cell format.
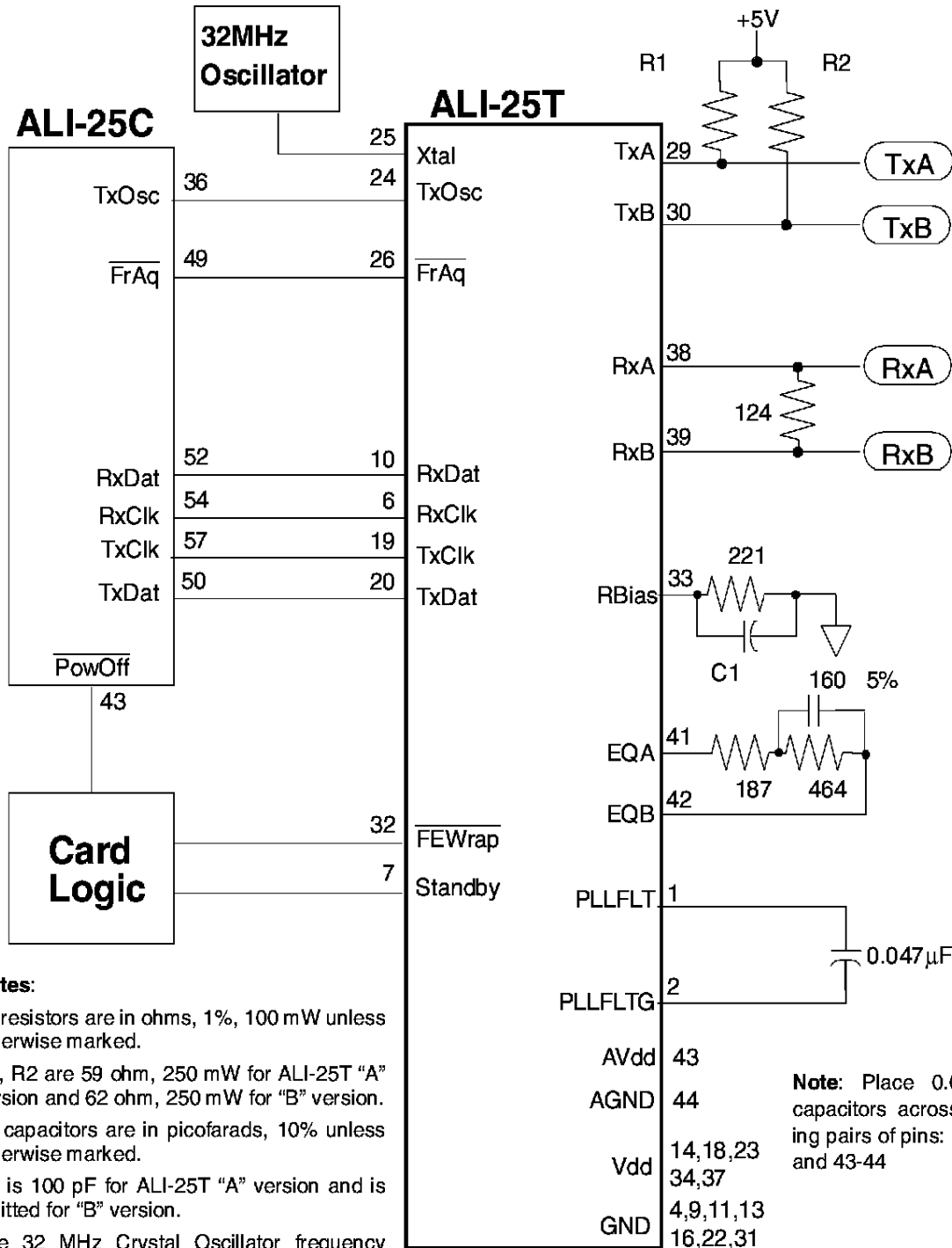
The ALI-25C does transmit the idle pattern following reset unless the Halt_Tx pin is high, which disables the ALI-25C transmitter. Prior to reset, the transmit function is not predictable except if it is disabled by the Halt_Tx pin being high.

The ALI-25C does not accept data transfers from the ATM Layer Protocol chip (SARA-S) and the TBClk output is held low until the ALI-25C Reset pin goes inactive.

CONNECTIONS

The ALI-25T and ALI-25C are operated as a pair in order to transmit and receive ATM cells over the connected network. There is, of course, another major component that is required: the transformer / filter that actually interfaces the line, which is called the Media Interface Magnetics Module (available from Pulse Engineering, Inc. as part number PE-67583 - call 619-674-8100 for information). The connections between the ALI-25C and the ALI-25T are illustrated in Figure 9, which also shows the line side analog component connections for the ALI-25T. The connections between the ALI-25T, the Magnetics Module and the line are illustrated in Figure 10.

Figure 9. ALI-25C and ALI-25T Connections

Notes:

All resistors are in ohms, 1%, 100 mW unless otherwise marked.

R1, R2 are 59 ohm, 250 mW for ALI-25T "A" version and 62 ohm, 250 mW for "B" version.

All capacitors are in picofarads, 10% unless otherwise marked.

C1 is 100 pF for ALI-25T "A" version and is omitted for "B" version.

The 32 MHz Crystal Oscillator frequency must be ± 100 ppm.

Note: Place 0.01μF (20%) capacitors across the following pairs of pins: 13-14, 22-23 and 43-44

The transformer / filter hybrid that must be used with the ALI-25T in order to properly interface with the transmission medium. The following diagram illustrates the transformer and connector that are recommended for use on the I/O of the ALI-25T.

Figure 10. Media Interface Magnetics Module Connections
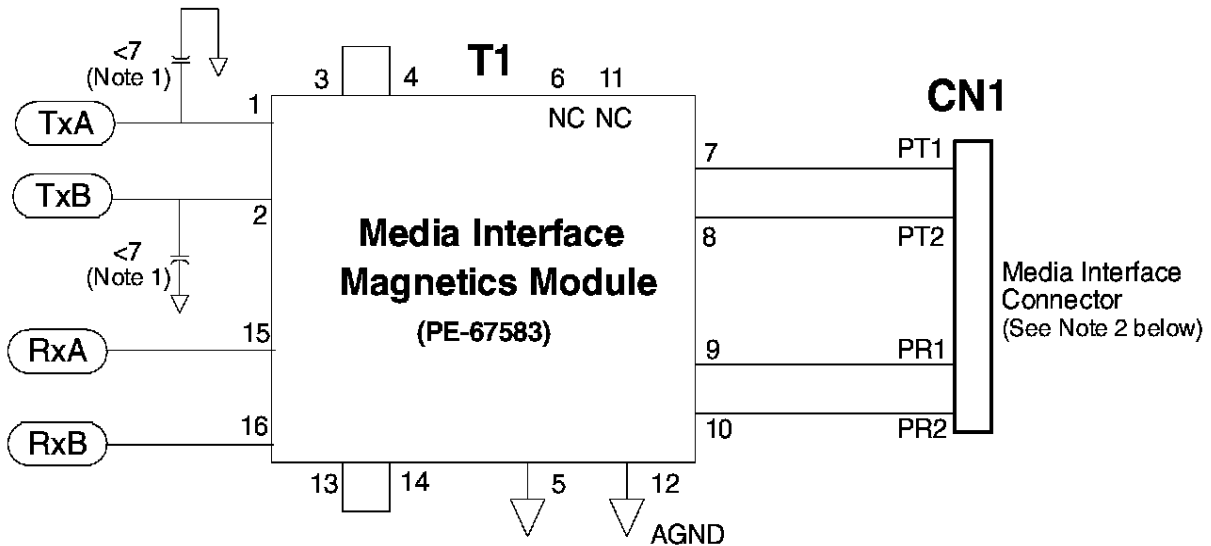
Notes:
1. The two capacitors designated <7 (picofarads) are used for radiation suppression and they should not be needed. It is recommended, however, that the wiring and pads for these components be placed on the card as a backup in case of EMC problems. Note that if these capacitors are used, they must be less that 7 pF to avoid transmission degradation.
2. The RJ45 connector is an acceptable media interface connector provided that the placement and wiring is done properly. The D-Shell connector is also acceptable and provides superior electrical characteristics.

Connector Pin Use for Concentrator/Hub/Switch Port

Station Port Signal Name	D-Shell Pins	RJ45 Pins
PR1	5 (B)	1
PT1	1 (R)	7
PT2	6 (G)	8
PR2	9 (O)	2

Connector Pin Use for PC/WorkStation Port

Station Port Signal Name	D-Shell Pins	RJ45 Pins
PT1	5 (B)	1
PR1	1 (R)	7
PR2	6 (G)	8
PT2	9 (O)	2
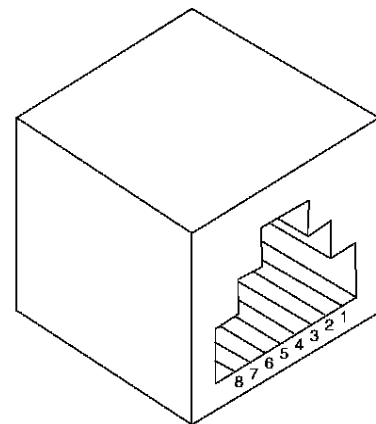
RJ45 Connector

PHYSICAL DESIGN

Introduction

ATM adapter cards are sensitive to physical layout in two areas: logic-switching noise immunity and electro-magnetic interference. Every effort should be made to optimize the physical layout of adapter cards for best operating performance. The following guidelines will assist the card designer in placing the components and connections, and in prioritizing the position of the wiring nets.

These guidelines have been developed through experience and theoretical analysis. Most of these will be recognized simply as good design practice applied specifically to this application. Unfortunately, they cannot, by themselves, guarantee correct operation, which must be verified by testing.

Noise Sources

The dominant noise source is the ALI-25T transmitter, which consists of the total circuit path from ALI-25T Tx A/B through the transformer(s) and out to the cable connector, including all components attached to these circuits. The 32-MHz crystal oscillator for the ALI-25T/ALI-25C is the second largest noise source. Special care must be taken to isolate these sources from the sensitive circuits. Other crystal oscillators and ALL the logic circuitry on the card are also sources of noise, although of lesser importance.

Sensitive circuits

The most sensitive circuit is the PLL circuit in ALI-25T, which includes the RC circuits from PLLFLT to PLL-FLTG. Other sensitive circuits include the equalizer circuit, EQA and EQB pins, and the entire receive path, from the cable connector through the transformer/filter to the RxA and RxB pins.

The ALI-25T Transmitter RBias circuit is less sensitive to noise than the above circuits.

Analog Path Physical Layout and Isolated Regions

Figure 11 illustrates the proper physical layout of an ATM 25 Mbit/s Analog Front End. The components as well as the proper voltage/ground plane isolation are shown. There are three isolated regions: the main logic region, the receive region, and the connector region.

Figure 11. Example of Physical Layout of ALI-25T Analog Front End
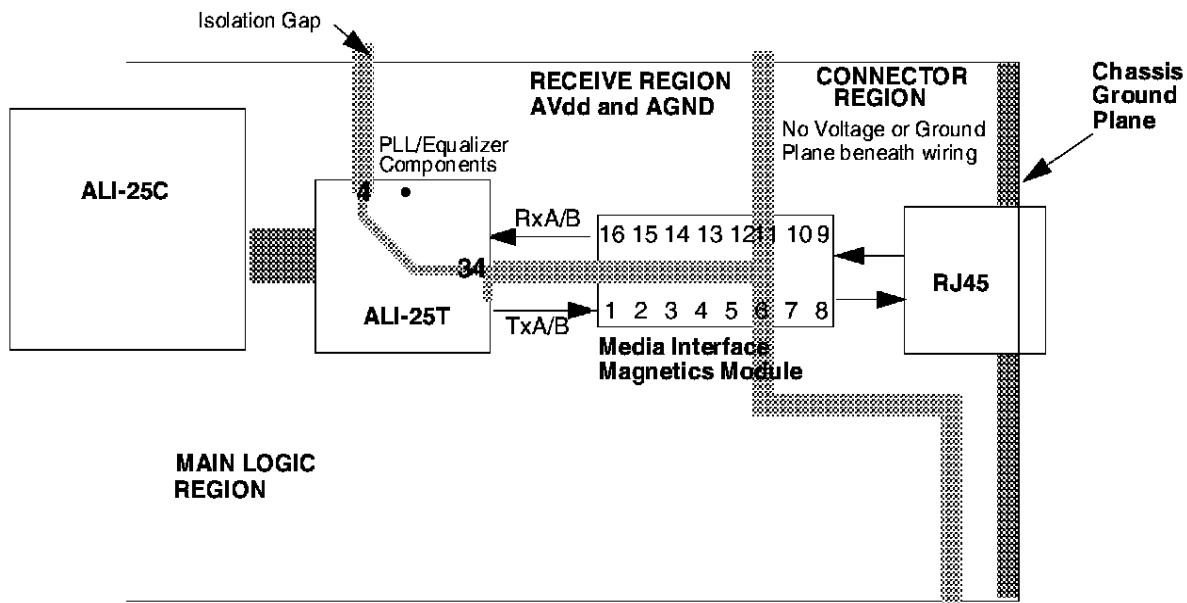
Main Logic Region

This region includes everything except the analog. The card power supply pins and the crystal oscillators should be in this region. In addition, the transmit path (including pins 1, 2, 3, 4, and 5 of the filter and transformer module), and the RBias circuit are placed over this main logic region. The transmit path is usually placed on the ground plane side of the card, and is best if on the signal plane closest to the ground plane

With the exception of the transmit, and the crystal oscillator, this region can use an automatic wiring program. Remember that the program must be blocked from wiring into the other regions.

ALI-25T Receive Region

This region includes the PLL circuit, the equalizer, and the receive path, including the transformer/filters. Usually the PLL circuit is placed on the ground plane side of the card, while the receive path is on the voltage side.

This region contains pins 13, 14, 15, and 16 of the transformer/filter module and extends underneath ALI-25T pins 1 through 3 and 35 through 44. ALI-25T pins 4 and 34 may sit in the gap.

Connector Region

This region of the plane has no underlying ground or voltage plane; it contains the connector and pins 7, 8, 9, and 10 of the transformer/filter module. The connector should be placed physically close to and in-line with the transformer/filter module. The receive and the transmit paths through these components should be symmetrical and should not be disturbed by unnecessary vias, test points, or changes in signal layers. This will maintain the common mode balance between the two pairs.

Proper Isolation of Regions

The following guidelines should be followed for the layout of the isolated regions, in particular the receive region.

• Electrically isolate regions of the power and ground planes by gaps or "moats" between the regions. The gaps should be 0.1" wide wherever possible (unlikely underneath components) and must be coincident on all voltage and ground planes.

• The receive region's power and ground should be supplied with zero-ohm resistors. Placement of these supply resistors should be towards the card power supply pins, but away from any noise source. The zero-ohm resistor circuit should not be placed close to the 0.047 μF PLL filter capacitor (see Figure 9).

• Decoupling capacitors (0.1μF) should be placed between Vdd and ground, and between AVdd and AGND. The decoupling should be physically located next to the zero ohm supply resistors, as shown in Figure 12. This decoupling is in addition to the three 0.01μF capacitors required for the ALI-25T (see Figure 9).

Figure 12. Connections Between Analog and Digital Vdd and GND
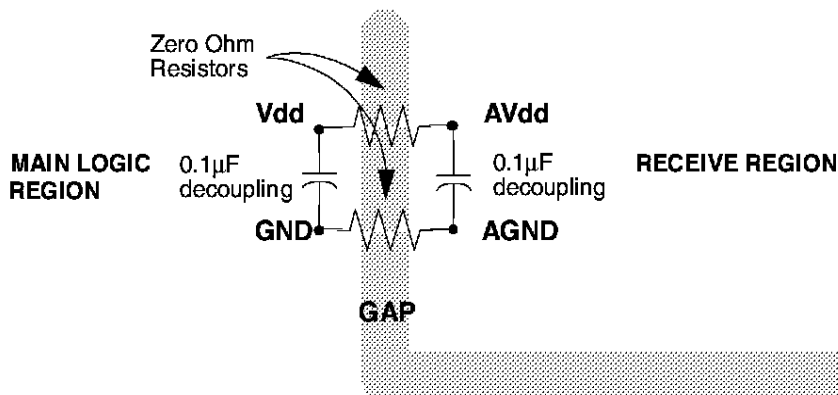
The following guidelines should be observed for wiring and placement in order to provide the greatest electrical isolation between circuits.

• Spatial separation - keep the components and wires far apart; and if the signal paths must cross, do so at right angles.

• Voltage plane sides - keep the components and wires for different circuits on opposite sides of the power/ ground planes. Each pin-through-hole or via will degrade this type of isolation, so minimize these.

WIRING GUIDELINES

Differential Pairs

The transmit path, receive path, and phantom drive path each constitute a differential pair. The signals on these lines are balanced, and referenced to each other, not to ground. These signals must be run in the same channel and there should be no vias between them. Also, these lines must be kept symmetric, for example, any routing or connection to one line should be complimentary with the other line. For example, these lines should not be run within 0.1" of a ground plane edge, because this would disturb the closer line more than the further line.

Because of the NRZI coding scheme, the wires in these differential pairs may be interchanged with no effect on the performance. This provides the physical designer with added flexibility to preserve the "good" routing. For example, if the routing from the transformer to TxA naturally runs to TxB, go ahead and swap TxA with TxB.

Analog circuits

The essence of analog wiring is to keep the area enclosed by a circuit loop as small as possible. This can conflict with the older, simpler rule of keeping line lengths small. For example, if components in the circuit are positioned along three sides of a square, the best return wiring would be back along the same three sides of the square, NOT directly back along the fourth side. This rule must be carried to extremes! There should never be an unnecessary pop-up or via inside the loop. This also means that the loop should never encircle the power/ ground planes, for example, part of the loop above and part below these planes.

Power Supply Decoupling Guidelines

On the ALI-25T, pins 22 and 23, pins 44 and 43, and pins 14 and 13, form supply points for separate groups of circuits. These pairs should each be decoupled with $0.01\mu F$. The connection to the power or ground plane should be at the module pin, with dedicated wires to the decoupling capacitor.

The power entry to the Receive Region should be decoupled as shown in Figure 12.

For the remainder of the card, "normal" decoupling guidelines apply. For example, a large (20 μF) cap in parallel with a small (0.01 μF) cap at the power entry onto the card is recommended. A small capacitor ($0.01\mu F$) wired between the Vdd and ground pins of the fast switching modules (like the crystal oscillator) is also recommended.

PACKAGE INFORMATION

ALI-25C

The ALI-25C is packaged in a 68-pin plastic leaded chip carrier (68 PLCC) that is suitable for socket or surface mounting, as shown in Figure 13. All dimensions shown are in millimeters and are nominal unless otherwise indicated.
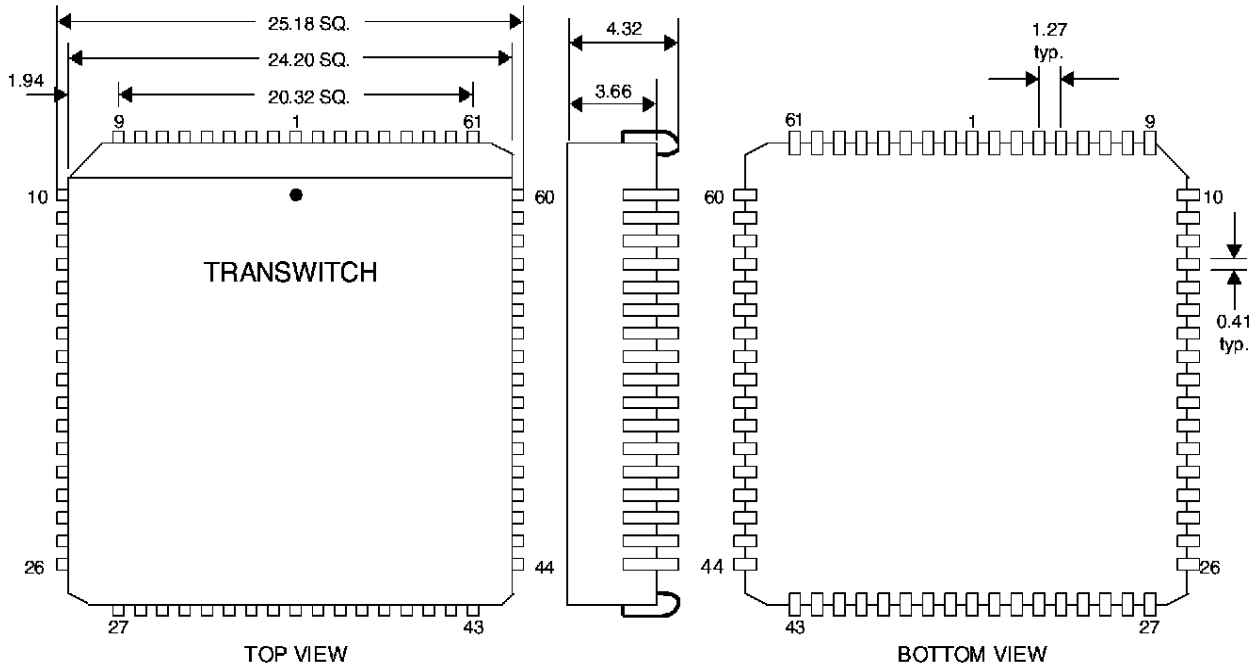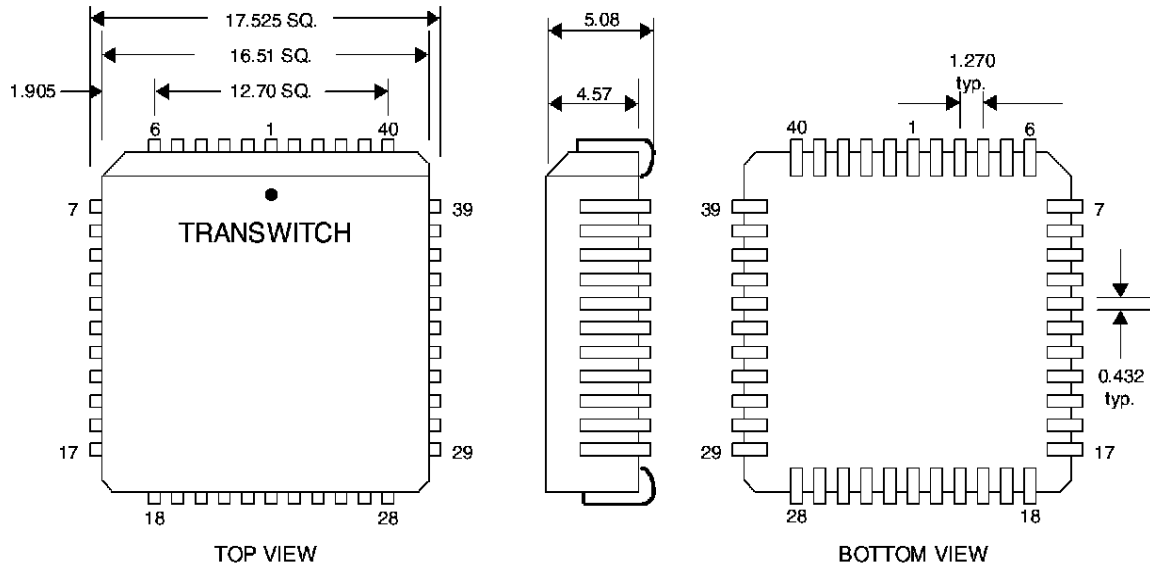

Figure 13. ALI-25C TXC-07125 68-Pin Plastic Leaded Chip Carrier

PACKAGE INFORMATION

ALI-25T

The ALI-25T is packaged in a 44-pin plastic leaded chip carrier (44 PLCC) that is suitable for socket or surface mounting, as shown in Figure 14. All dimensions shown are in millimeters and are nominal unless otherwise indicated.

Figure 14. ALI-25T TXC-07225 44-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

ALI-25C Controller Chip

Part Number: TXC-07125-ACPL

ALI-25T Transceiver Chip

"A" version   Part Number: TXC-07225-ACPL
"B" version   Part Number: TXC-07225-BCPL

RELATED PRODUCTS

TXC-05501/05601 SARA-S and SARA-R Devices. These TranSwitch products satisfy all requirements for ATM layer processing of cells including AAL3/4, AAL5 and Constant Bit Rate applications. These chips interface directly with the ALI-25 chip set.

TXC-05801 CUBIT VLSI Device. A *CellBus* - based ATM cell switching device.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-TSS (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (TSS)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within the updated ALI-25 Data Sheet that have significant differences relative to the superseded ALI-25 Data Sheet:

Updated ALI-25 Data Sheet: Edition 3A, August 1996

Superseded ALI-25 Data Sheet: Edition 3, October 1995

The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Updated edition number and date.
1	Modified the last item of Feature list to include "A" and "B" versions of the ALI-25T device.
2	Updated Table of Contents and List of Figures.
5	Moved the location of Block Diagram Description (ALI-25T) section. Added first sentence to the first paragraph and added the second paragraph to Block Diagram Description (ALI-25T) section.
25	Modified Figure 9 resistor and capacitor details.
26	Modified Figure 10 to include RJ45 connector diagram.
32	Modified the second item of Ordering Information section.
34	Updated List of Data Sheet Changes.
37	Updated Documentation Update Registration Form.

- NOTES -

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DOCUMENTATION UPDATE REGISTRATION FORM

If you would like be added to our database of customers who have registered to receive updated documentation for this device as it becomes available, please provide your name and address below, and fax or mail this page to Mary Lombardo at TranSwitch. Mary will ensure that relevant Product Information Sheets, Data Sheets, Application Notes, Technical Bulletins and other relevant publications are sent to you. This information will be made available in paper document form, on a Windows/DOS/Macintosh/UNIX CD-ROM disk, and on the Internet World Wide Web at the TranSwitch site, http://www.transwitch.com.

Please print or type the information requested below, or attach a business card.

Name: _____

Title: _____

Company: _____

Dept./Mailstop: _____

Street: _____

City/State/Zip: _____

If located outside U.S.A., please add - Postal Code: _____ Country: _____

Telephone:_____ Ext.: _____

Fax: _____ E-Mail: _____

Purchasing Dept. Location: _____

Check a box if your computer has a CD-ROM drive: DOS ❑ Windows ❑ Mac ❑   UNIX ❑ ↓

Check box if you have Internet Web access: ❑   Sun ❑ Solaris ❑ HP ❑ Other ❑

Please describe briefly your intended application for this device, and indicate whether you would care to have a TranSwitch applications engineer contact you to provide assistance:

_____

_____

_____

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If you are also interested in receiving updated documentation for other TranSwitch device types, please list them below rather than submitting separate registration forms:

_____ _____ _____ _____ _____ _____

Please fax this page to Mary Lombardo at (203) 926-9453 or fold, tape and mail it (see other side)

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8 Progress Drive
Shelton, CT 06484
U.S.A.

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